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09/476,678	12/30/1999	PHILIP NORD JENKINS	499.028US1	8138

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
MUNOZ, GUILLERMO	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 02/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/476,678	Applicant(s) JENKINS ET AL.	
	Examiner Guillermo Munoz	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-8, 10-15, 21-31, and 37-42* is/are rejected.

7)☒ Claim(s) *5,9,16-20 and 32-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

The drawings filed on 12/30/99 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-8, 10-15, 21-31, and 37-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishibashi et al (US Patent Number 5621774) in view of Taya et al (US Patent Number 5778214), Konno (US Patent Number 5537068), and Gervasi (US Patent Number 5948083).

In regards to claim 1; Ishibashi et al teaches a method of reducing skew between a plurality of signals transmitted with a transmit clock wherein:

- "DT(0) to DT(n) represent data, CK represents the data write control signal such as the clock, and L_{in} (0) to L_{in} (n)"(col.7, lines 37-39).

The received signals D(0) to D(n) and CK are equivalent to claimed receiving the transmit clock and each of the plurality of signals in claim 1, line 4.

- "At this state, the data DT(0) to DT(n) and the signal CK are input from the transmitting circuit as a one-pulse signal. Outputs of the latch circuits $L_{in\,(0)}$ to $L_{in\,(n)}$ are then examined and unfixed selection signals SEL0(i) to SELn(k) are decremented"(col.7, lines 58-62).

The examination of the outputs of the latch circuits is equivalent to claimed detecting skew between the received transmit clock and each of the received signals in claim 1, lines 5-6.

The decrementing of the selection signals of the bits that may be latched is equivalent to claimed adding delay to one or more of the plurality of received signals to compensate for the detected skew in claim 1, lines 7-8.

Ishibashi et al teaches increasing the cycle time tcyc, thus the valid area tw of data is increased and there is a possibility of attaining the data transfer, even when the skew of the data and clock to be transferred is increased. However, Ishibashi et al fails to teach readjusting the delay of the data signals as a means to compensate for increased skew.

Taya et al teaches another means for compensating for increased skew in a delayed data signal skew compensation system wherein:

- "The bit-phase adjusting circuit 1 adjusts a phase difference between the data signals and the clock signal by adjusting a delay of the data signal"(col.4, lines 37-39).
- "While it is desired that the data signal is to be transmitted without error for a long time after the bit-phase aligning circuit enters the synchronous state, the phase relationship between the input data signal and the input clock signal may change due to, for example, a temperature variation. As appreciated, the bit-phase aligning circuit of this embodiment can adapt to such a change of the phase relationship with an adaptive range or width

which depends on the forgoing phase adjustable range or width of the variable delay circuit 11"(col.7, lines 9-18).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to compensate for increased skew in the receiver taught by Ishibashi by adjusting the variable delay of the data signals in view of Taya for the purpose of maintaining the phase relationship between the clock signal and the data signals.

In regards to claims 3 and 8; as applied to claims 2 and 7, Ishibashi teaches a circuit and method of circuit for reducing skew between a plurality of signals transmitted with a transmit clock wherein:

- "input data DT(0) to DT(n) delayed by a variable delay circuit 0 designated by VD(0) to a variable delay circuit n designated by VD(n) in response to the CK"(col.7, lines 39-41).

The variable delay lines VD(0)...V(n) are equivalent to claimed separate delay lines in claims 3 and 8.

In regards to claim 10, 12, and 28; as applied to claims 1, 11, and 27, respectively, Ishibashi teaches a circuit and method of circuit for reducing skew between a plurality of signals transmitted with a transmit clock wherein:

- "DT(0) to DT(n) represent data, CK represents the data write control signal such as the clock, and L_{in} (0) to L_{in} (n) the latch circuits for latching"(col.7, lines 37-39).

Data latches L_{in} (0) to L_{in} (n) are functionally equivalent to claimed output register in claims 10, 12, and 28.

In regards to claims 11, 27, and 39 and in regards to claims 6, 13, and 29; as applied to claims 1, 11, and 27, respectively, Ishibashi et al teaches a circuit for reducing skew between a plurality of signals transmitted with a channel clock comprising:

- "DT(0) to DT(n) represent data, CK represents the data write control signal such as the clock, and L_{in} (0) to L_{in} (n) the latch circuits for latching the input data DT(0) to DT(n) delayed by a variable delay circuit 0 designated by VD(0) to a variable delay circuit n designated by VD(n) in response to the CK. A variable delay control circuit 81 produces selection signals SEL0(i) to SELn(k) for the variable delay circuits 0 to n in accordance with outputs of the latch circuits L_{in} (0) to L_{in} (n) and controls delay times of the variable delay circuits 0 to n in accordance with the selection signals SEL(i) to SEL(k)"(col.7, lines 36-47).

The latch L_{in} (0) and variable delay circuit VD(0) are equivalent to claimed first data capture circuit connected to the first signal, wherein the first data capture circuit includes a first delay line and a first skew detection circuit connected to the first delay line in claim 11, lines 4-6; claim 27, lines 6-8; and claim 39, lines 6-8.

The latch L_{in} (n) and variable delay circuit VD(n) are equivalent to claimed second data capture circuit connected to the second signal, wherein the second data capture circuit includes a second delay line and a second skew detection circuit connected to the second delay line in claim 11, lines 7-9; claim 27, lines 9-11; and claim 39, lines 9-11.

- "A variable delay control circuit 81 produces selection signals SEL0(i) to SELn(k) for the variable delay circuits 0 to n in accordance with outputs of the latch circuits L_{in} (0) to L_{in}

(n) and controls delay times of the variable delay circuits 0 to n in accordance with the selection signals SEL(i) to SEL(k)"(col.7, lines 43-47).

The control circuit 81 is equivalent to claimed delay line controller connected to the first and second delay lines and the first and second skew detection circuits, wherein the delay line controller receives skew indicator signals representing skew from each of said first and second skew detection circuits and controls delay added by said first and second delay lines in claim 11, lines 10-13; claim 27, lines 12-16; and claim 39, lines 12-16.

Ishibashi et al teaches the data signals DT(0) to DT(n) are latched into latch circuits L_{in} (0) to L_{in} (n) in response to clock signal CK. Ishibashi et al does not particularly call for doubling the frequency of clock signal CK. However, Ishibashi et al does teach consideration of the timing of the clock when transmitting between apparatuses.

Konno discloses problems associated with the timing of an externally supplied clock wherein:

- "At the higher clock rates of modern microprocessors (50 to 100 MHz), the distribution of a CLK 2 signal with a 100 to 200 MHz rate presents difficult design problems due to the complexity that requires substantial skills in high frequency analog techniques. Also, simple circuits, such as CLKDRV 19, have delays of 2 to 3 ns which are significant when compared with the periods of 50 to 100 MHz clocks. The use of 1X external clock is precluded by the need to generate a 50% duty cycle on-chip clock. In fact, it would be preferable to use an external clock with a one-half rate (2X) for reduced distribution problems if a 1X clock signal with a 50% duty cycle could be readily generated on-chip"

Konno, further, teaches circuits and circuit methods for improve timing of clock signals when transmitted between apparatuses wherein:

- "A tapped delay-line is used to synthesize a 50% duty cycle clock waveform form an externally supplied clock signal in a feed-forward circuit configuration. The synthesized clock waveform may have a clock rate of one-half, the same, or twice the externally supplied clock"(col.2, lines 61-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to multiply the clock signal CK taught by Ishibashi et al at the receiving apparatus using a tapped delay-line in view of Konno for the purpose of avoiding undesired delay in the transmission of the clock signal from one apparatus to another.

In regards to claims 22 and 38; Ishibashi et al teaches a circuit for reducing skew between a plurality of signals transmitted with a transmit clock wherein:

- "technique for transferring data between apparatuses such as work stations and computers"(col.1, lines 7-8).

However, Ishibashi et al fails to teach a clock signal generated from a core clock generator of a computer.

Konno teaches another computer system wherein:

- "Synchronous operation of the various units in the microprocessor system is accomplished by means of the clock (CLK) signal. Each unit uses the CLK signal for sequencing the operation of internal sequential logic circuits such as synchronous state machines. Inside CPU 11, CLK is generated by the clock generator circuit (CLKGEN) 17"(col.1, lines 23-28).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to generate the clock signal CK taught by Ishibashi et al using a CPU system clock generation unit in view of Konno for the purpose of maintaining system wide syncronization.

In regards to claim 23 and in regards to claims 2, 7, 21, and 37; as applied to claims 1, 6, 11, and 27, respectively, Ishibashi et al teaches a circuit for reducing skew between a plurality of signals transmitted with a transmit clock wherein:

- "a variable delay control circuit for controlling the delay amount of the variable delay circuits by means of output signals of the latch circuits"(col.2, lines 35-37).
- "The variable delay control circuit divides the data into n/m by means of the arrival time of data to the receiving apparatus and controls the delay times of the variable delay circuits so that m data can be latched by the latch circuits. The timing chart in the case of m=n/2 is as shown in FIG. 13. The n/2 received data 1 arriving early at the receiving apparatus is latched by the received clock 1 and the remaining n/2 received data 2 is latched by the received clock 2"(col.2, lines 57-64).

Ishibashi et al does not particularly call for a circuit wherein: "the phase comparator compares phase of an input signal to a clock signal to generate a clock early signal and a data early signal." However, Ishibashi et al does teach that the variable delay control circuit adjust the amount of delay applied to the data signal by applying selection signals to each data line based upon the arrival time of the data with respect to the clock.

Gervasi teaches another circuit for detecting the arrival time of a data signal wherein:

- "When an input data signal is received along the input data line, it is passed on to each of the data latches. Each data latch outputs the data based upon a strobe signal received from the associated delay block. The result is oversampling the input data signal to determine whether the input data signal is early, on-time, or late"(col.2, lines 64-68 & col.3, lines 1-2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adjust the phase of the data signal of Ishibashi et al based upon generated early data signal and a data late signal in view of Gervasi for the purpose of reducing skew in the received data signals.

In regards to claim 24; as applied to claim 23 above, Ishibashi et al teaches a circuit for reducing skew between a plurality of signals transmitted with a transmit clock wherein:

- "L_{in} (0) to L_{in} (n) the latch circuits for latching the input data DT(0) to DT(n) delayed by a variable delay circuit 0 designated by VD(0) to a variable delay circuit n designated by VD(n) in response to the CK"(col.7, lines 38-41).

The latch circuits are equivalent to claimed plurality of flip-flops in claim 24.

In regards to claims 14, 15, 25, and 31; Ishibashi et al teaches a delay line controller for controlling a plurality of delay lines wherein:

- "A variable delay control circuit 81 produces selection signals SEL0(i) to SELn(k) for the variable delay circuits 0 to n in accordance with outputs of the latch circuits L_{in} (0) to L_{in} (n) and controls delay times of the variable delay circuits 0 to n in accordance with the selection signals SEL(i) to SEL(k)"(col.7, lines 43-47).

The outputs of latch circuits L_{in} (0) to $L_{in\,is}$ equivalent to claimed plurality of skew indicator signals inputs, wherein each skew indicator signal input is capable of receiving a skew indicator signal reflecting skew between one of the delayed input signals and a reference signal in claim 25, lines 4-6.

The variable delay control circuit 81 is equivalent to claimed control logic for controlling the plurality of delay lines as a function of the delay control signals in claim 25, lines 10-11.

Ishibashi et al does not particularly call for a circuit wherein: "a digital filter connected to each of said plurality of skew indicator signal inputs, wherein each digital filter generates a delay control signal associated with one of the delayed input signals." However, Ishibashi et al does teach "variable delay control circuit gradually reduces the delay time of the variable delay circuits for respective data and completes control of the variable delay circuits when the latch circuits can be latched"(col.3, lines 15-18).

Konno teaches another means for gradually applying a control signal wherein:

- "Low-pass filter (LPF 22) smoothes the output of CP 21 before applying the control signal to VCO 23"(col.2, lines 5-7).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to gradually reduce the delay time of the variable delay circuit taught by Ishibashi by passing the selection signal through a low-pass filter in view of Konno for the purpose of controlling the rate of change of delay applied to the data signal.

In regards to claim 26; as applied to claim 25, Ishibashi et al

- "A variable delay control circuit 81 produces selection signals SEL0(i) to SELn(k) for the variable delay circuits 0 to n in accordance with outputs of the latch circuits L_{in} (0) to L_{in}

(n) and controls delay times of the variable delay circuits 0 to n in accordance with the selection signals SEL(i) to SEL(k)"(col. 7, lines 42-46). The delay control circuit, latch circuits, and variable delay circuits are equivalent to claimed feedback control system which adaptively deskews the input signals.

In regards to claim 40; as applied to claim 11 above, Ishibashi et al teaches a method for establishing phase relationship between a plurality of signals and a reference signal wherein:

- "Further, the data and CK to be transferred during the adjustment use the pulse signals of one-pulse signal, a predetermined pattern may be transferred"(col.5, lines 48-51).

The method of transferring the pulse signals of one-pulse signal comprising a predetermined pattern is equivalent to claimed initializing signal deskewing circuitry, wherein initializing includes driving the circuitry with a predefined sequence of data edges in claim 40, lines 3-4.

- "Outputs of the latch circuits L_{in} (0) to L_{in} (n) are then examined and unfixed selection signals SEL0(i) to SELn(k) are decremented"(col.7, lines 60-62).

The latch circuits are equivalent to claimed phase comparator in claim 40, line 5.

Ishibashi et al does not particularly call for a method wherein: "driving the phase comparator with a clock having 2 edges per data bit". However, Ishibashi et al does teach "The n/2 received data 1 arriving early at the receiving apparatus is latched by the received clock 1 and the remaining n/2 received data 2 is latched by the received clock 2"(col.2, lines 62-64).

Gervasi teaches another method of latching received data wherein:

- "The present invention advantageously oversamples the input data signal to virtually guarantee data capture. Oversampling the input data signal allows for beneficially monitoring the input data signal as a data strobe signal is triggered at various intervals when latching the input data signal"(col.7, lines 27-31).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to latch the received data signal taught by Ishibashi et al using clock 1 and clock 2 samples in view of Gervasi for the purpose of eliminating minor skew conditions.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 42 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 42 recites the phrase "initializing a DMC value for each channel signal". It is suggested the acronym DMC be defined.

Claim Objections

Claims 5, 9, 16-20, and 32-36 are objected to as being dependent upon a rejected base claims 3, 7, 11 and 27, respectively, but would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guillermo Munoz whose telephone number is 703-305-4224. The examiner can normally be reached on Monday-Friday 8:30a.m-4:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9313 for regular communications and 703-872-9313 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

Guillermo Munoz

GM
February 21, 2003

STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600